Electronic Version
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Claims

[c1] 1. A method for analyzing the timing of a circuit, comprising:

determining at least one location information for one or more inputs to a timing test; and

computing a timing slack for the timing test using the at least one location information.

[c2] 2. The method of claim 1, wherein the input to a timing test is a path or a logic cone.

[c3] 3. The method of claim 1, wherein the at least one location information comprises a bounding region for the one or more inputs to the timing test.

[c4] 4. The method of claim 3, wherein said determining comprises defining the bounding region based on the locations of the one or more inputs to the timing test.

[c5] 5. The method of claim 4, wherein said determining further comprises modifying a size of the bounding region to account for variations in delay among the one or more inputs to the timing test.

[c6] 6. The method of claim 5, wherein said computing com-

prises:

determining a slack variation factor based on the size of the bounding region; and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test.

[c7] 7. The method of claim 1, wherein the at least one location information comprises a centroid of the one or more inputs to the timing test.

[c8] 8. The method of claim 7, wherein the centroid comprises the averaged location of the one or more inputs to the timing test.

[c9] 9. The method of claim 7, wherein the centroid comprises the delay-weighted averaged location of the one or more inputs to the timing test.

[c10] 10. The method of claim 7, wherein said determining comprises:

calculating a first centroid of a first input to the timing test;

calculating a second centroid of a second input to the timing test; and

determining the distance between the first and second centroids.

[c11] 11. The method of claim 10, wherein said calculating comprises:

determining a slack variation factor based on the distance between the first and second centroids; and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test.

[c12] 12. The method of claim 1, wherein the at least one location information comprises an abstract location information.

[c13] 13. The method of claim 12, wherein the abstract location information is based upon correlation of delay functions.

[c14] 14. A computer-readable medium containing instructions that, when executed, cause a computer to:

determine at least one location information for one or more inputs to a timing test; and

compute a timing slack for the timing test using the at least one location information.

[c15] 15. The medium of claim 14, wherein the input to a timing test is a path or a logic cone.

[c16] 16. The medium of claim 14, wherein the at least one lo-

cation information comprises a bounding region for the one or more inputs to the timing test.

[c17] 17. The medium of claim 16, wherein said determining comprises defining the bounding region based on the locations of the one or more inputs to the timing test.

[c18] 18. The medium of claim 17, wherein said determining further comprises modifying a size of the bounding region to account for variations in delay among the one or more inputs to the timing test.

[c19] 19. The medium of claim 18, wherein said computing comprises:

determining a slack variation factor based on the size of the bounding region; and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test.

[c20] 20. The medium of claim 14, wherein the at least one location information comprises a centroid of the one or more inputs to the timing test.

[c21] 21. The medium of claim 20, wherein the centroid comprises the averaged location of the one or more inputs to the timing test.

[c22] 22. The medium of claim 20, wherein the centroid comprises the delay-weighted averaged location of the one or more inputs to the timing test.

[c23] 23. The medium of claim 20, wherein said determining comprises:

calculating a first centroid of a first input to the timing test;

calculating a second centroid of a second input to the timing test; and

determining the distance between the first and second centroids.

[c24] 24. The medium of claim 23, wherein said computing comprises:

determining a slack variation factor based on the distance between the first and second centroids; and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test.

[c25] 25. The medium of claim 14, wherein the at least one location information comprises an abstract location information.

[c26] 26. The medium of claim 25, wherein the abstract location information is based upon correlation of delay func-

tions.

[c27] 27. A method of analyzing the timing of an integrated circuit, comprising:

identifying an early path and a late path in the integrated circuit;

determining a timing slack variation in the early path using location information on one or more elements in the early path;

determining a timing slack variation in the late path using location information on one or more elements in the late path; and

computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path.

[c28] 28. The method of claim 27, wherein the location information on the one or more elements in the early path and the location information on the one or more elements in the late path comprise bounding regions defined around the one or more elements in the early path and the one or more elements in the late path, respectively.

[c29] 29. The method of claim 27, wherein the location information on the one or more elements in the early path

and the location information on the one or more elements in the late path comprise centroids calculated by considering the one or more elements in the early path and the one or more elements in the late path, respectively, as aggregates.

[c30] 30. The method of claim 27, wherein the method is performed for an early mode timing analysis of the integrated circuit and a late mode timing analysis of the integrated circuit.